~~a silicide layer disposed on said top and sidewalls of said polysilicon gate.~~

11. The transistor structure of claim 10 wherein said source/drain regions are aligned with a said sidewall of said polysilicon gate.

12. The transistor structure of claim 10 wherein said silicide layer is titanium silicide.

13. The transistor structure of claim 11 wherein said silicide layer is titanium silicide.

14. The transistor structure of claim 10 further including a lightly doped source/drain extension of each of said source/drain regions extending under said polysilicon gate.

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15. The transistor structure of claim 11 further including a lightly doped source/drain extension of each of said source/drain regions extending under said polysilicon gate.

16. The transistor structure of claim 12 further including a lightly doped source/drain extension of each of said source/drain regions extending under said polysilicon gate.

17. The transistor structure of claim 13 further including a lightly doped source/drain extension of each of said source/drain regions extending under said polysilicon gate.

18. The transistor structure of claim 10 further including a dielectric extending from said gate dielectric of increased thickness relative to said gate dielectric and disposed under said silicide layer.

19. The transistor structure of claim 11 further including a dielectric extending from said gate dielectric of increased thickness relative to said gate dielectric and disposed under said silicide layer.

20. The transistor structure of claim 12 further including a dielectric extending from said gate dielectric of increased thickness relative to said gate dielectric and disposed under said silicide layer.

21. The transistor structure of claim 13 further including a dielectric extending from said gate dielectric of increased thickness relative to said gate dielectric and disposed under said silicide layer.

22. The transistor structure of claim 14 further including a dielectric extending from said gate dielectric of increased thickness relative to said gate dielectric and disposed under said silicide layer.

23. The transistor structure of claim 15 further including a dielectric extending from said gate dielectric of increased thickness relative to said gate dielectric and disposed under said silicide layer.

24. The transistor structure of claim 16 further including a dielectric extending from said gate dielectric of increased thickness relative to said gate dielectric and disposed under said silicide layer.

25. The transistor structure of claim 17 further including a dielectric extending from said gate dielectric of increased thickness relative to said gate dielectric and disposed under said silicide layer.

26. The transistor structure of claim 10 wherein said silicide layer extends to said gate dielectric.